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#8 Declaration y Pierson 9/30/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Richard L. Pierson, Jr. et al. Examiner: Kang, Donghee

Serial No. 10/075,428 Art Unit: 2811

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For: HETEROJUNCTION BIPOLAR TRANSISTOR WITH InGaAs CONTACT AND ETCH STOP LAYER FOR InP SUB-COLLECTOR

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF RICHARD L. PIERSON, JR.

I, Richard L. Pierson, Jr., declare as follows:

1. I am a co-inventor of the above invention. At all times mentioned in this declaration, and continuing to the present, I have been a Research Scientist-Electronics for Rockwell Scientific Company, formerly known as Rockwell Science Center.
2. I cannot assign a specific date to the conception of the above invention. However, it occurred prior to February 7, 2001. On February 7, 2001 Rockwell ordered wafers from which samples of the invention could be completed from two vendors: Intelligent Epitaxy Technology, Inc., and IQE Inc. A copy of an internal Rockewell Scientific Center record documenting the order to Intelligent Epitaxy Technology is attached as Attachment 1. It shows that the order was requested by my co-inventor Berinder (B.) Brar on 2/6/01, and approved by various persons within Rockwell Science Center on 2/6/01 and 2/7/01. In the normal course of business, the order would have been telephoned to Intelligent Epitaxy Technology, Inc. on the same date as the last approval, with a written confirmation of the order sent either the same day or shortly afterward. At The same time, an order for additional wafers was placed with IQE Inc.

3. The order to Intelligent Epitaxy Technology, Inc. was filled on February 28, 2001, and to IQE Inc. on March 29, 2001, as evidenced by their shipping statements (Attachment 2). These statements show that the wafers included layers for an InP emitter, InGaAs base, InP collector, InGaAs etch stop/contact, and InP sub-collector and substrate.
4. Promptly upon receipt of the wafers, I requested scheduling by the Rockwell fabrication facility so that the wafers could be processed into working samples by appropriate etching and addition of contacts and metalization.
5. The wafers were processed over the period April 19 – June 7, 2001. During this time, active processing took place on a very frequent basis. Some of the process steps were documented by date, and other were not. Attachment 3 consists of copies of processing documentation, showing that active processing steps took place on at least the following dates: April 19, 20, 24, 26, 27 and 30, May 1, 2, 10, 11, 14, 15, 16, 25, 29, 30 and 31, and June 1, 3, 5, 6 and 7, 2001.
6. The resulting wafers were tested, with testing completed on or about June 11, 2001. The tests showed that the parts operated successfully as heterojunction bipolar transistors. Samples of the test results for the tests performed on the devices that were fabricated from wafers provided by IQE Inc. are attached as Attachment 4. The Common Emitter Output Curves at the lower right of these sheets in particular show successful transistor operation. Samples of test results for transistors fabricated from the wafers provided by Intelligent Epitaxy Technology, Inc. are attached in Attachment 5. These tests also showed successful transistor operation, although the base-emitter turn-on voltage was shifted from the desired level of 0.5 volts to about 0.7 volts, and there was also a poor yield. These defects were attributed to the base being doped with Be which diffused into the adjacent layers, primarily the emitter, rather than to any problem associated with the design of the invention itself. All of the samples had a structure shown and claimed in the above patent application.
7. The test results presented in Attachments 4 and 5 represent only a relatively small portion of the wafers that were tested. Additional wafer tests also showed that the fabricated devices exhibited successful transistor operation.

8. All of the documents attached to this declaration were generated contemporaneous with the dates indicated, and in the normal course of business.
9. I further declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true. These statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such willfull false statement may jeopardize the validity of this application or any patent issuing from this application.

Date: 9/10/03

Richard L. Pierson, Jr.

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